IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented): A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a drift layer of a first conductivity type formed on a first main surface of the semiconductor substrate, a surface of the drift layer having a first area and a second area which is positioned on an outer periphery of the first area;

a cell portion which is formed in the first area of the drift layer and includes a first base layer of a second conductivity type selectively formed in a surface layer of the first area, a source layer of a first conductivity type selectively formed in a surface layer of the first base layer, a first metallic compound which is formed on the surface layer of the first base layer and a surface layer of the source layer in common, and a control electrode which is formed in the first base layer and the source layer via a first insulating film and has a second metallic compound formed on a top surface thereof;

a terminating portion which is formed in the second area of the drift layer, alleviates an electric field to maintain a breakdown voltage by extending a depletion layer, and includes a second base layer of a second conductivity type selectively formed in a surface layer in the second area of the drift layer, an impurity diffused layer of a second conductivity type formed in a surface layer of the second base layer, and a third metallic compound which is provided to a surface layer of the impurity diffused layer, an end surface thereof on the terminating portion side being positioned on the cell portion side away from an end surface of the impurity diffused layer on the terminating portion side;

a first main electrode formed so as to be in contact with the first metallic compound and the third metallic compound in common; and a second main electrode formed on a second main surface opposite to the first main surface of the semiconductor substrate.

2. (Previously Presented): The semiconductor device according to claim 1, further comprising a second insulating film which is formed in the second area of the drift layer and on a further peripheral area surface of the terminating portion side end surface of the third metallic compound,

wherein the impurity diffused layer is formed in a self-alignment manner with respect to an end portion of the second insulating film on the cell portion side.

3. (Previously Presented): The semiconductor device according to claim 2, wherein the second insulating film is formed thicker than the first insulating film.

4. (Previously Presented): The semiconductor device according to claim 1, further comprising a second insulating film which is formed thicker than the first insulating film in the second area of the drift layer and outside of the third metallic compound,

wherein the impurity diffused layer is formed in a self-alignment manner with respect to an end portion of the second insulating film on the cell portion side.

5. (Previously Presented): The semiconductor device according to claim 1, wherein the second insulating film has a first side wall spacer formed on an end surface thereof on the cell portion side, and

the third metallic compound is formed in a self-alignment manner with respect to the first wall spacer.

6. (Previously Presented): The semiconductor device according to claim 1, further comprising a third insulting film which is formed on a surface of an end portion of the impurity diffused layer on the terminating portion side and has a thickness which allows passage of a second conductivity type impurity to form the impurity diffused layer.

7. (Previously Presented): The semiconductor device according to claim 1, wherein the control electrode is formed so as to have a stripe planar shape, and

a distance between an end surface of the third metallic compound on the terminating portion side and an end surface of the impurity diffused layer on the terminating portion side is assured by a diffusion depth of the impurity diffused layer in a direction orthogonal to a longitudinal direction of the stripe of the control electrode and a width of the first side wall spacer.

8. (Previously Presented): The semiconductor device according to claim 1, wherein a distance between the end surface of the third metallic compound on the terminating portion side and an end surface of the impurity diffused layer on the terminating portion side is equal to or more than 0.2 μm.

9. (Previously Presented): The semiconductor device according to claim 1, further comprising a second side wall spacer provided on a side surface of the control electrode,

wherein the first metallic compound and the second metallic compound are insulated from each other by the second side wall spacer.

10. (Previously Presented): The semiconductor device according to claim 9, wherein the second metallic compound is extended onto the second side wall spacer.

11. (Previously Presented): The semiconductor device according to claim 1, further comprising a fourth metallic compound formed on a top face of the field plate electrode.

12. (Previously Presented): The semiconductor device according to claim 2, wherein to the field plate electrode is applied substantially the same potential as that of the first main electrode or the control electrode.

13. (Previously Presented): A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a drift layer of a first conductivity type formed on a first main surface of the semiconductor substrate and has a first area and a second area which is positioned on an outer periphery of the first area;

a cell portion which is formed in the first area of the drift layer, and includes a first base layer of a second conductivity type selectively formed in a surface layer of the first area, a trench formed so as to extend from a surface of the first base layer to the inside of the drift layer, a first insulating film formed on a bottom surface and side surfaces of the trench, a source layer of a first conductivity type selectively formed in a surface layer of the first base layer so as to be in contact with the first insulating film, a first metallic compound formed on a surface of the first base layer and a surface of the source layer in common, and a control electrode which is formed so as to fill the trench via the first insulating film and has a second metallic compound formed on a top face thereof;

a terminating portion which is formed in the second area of the drift layer and alleviates an electric field to maintain a breakdown voltage by extending a depletion layer, and includes a second base layer of a second conductivity type selectively formed in a surface layer in the second area of the drift layer, an impurity diffused layer of a second conductivity type formed in a surface layer of the second base layer, and a third metallic compound which is formed in a surface layer in the impurity diffused layer, an end surface thereof on the terminating portion side being positioned on the cell portion side away from an end surface of the impurity diffused layer on the terminating portion side;

a first main electrode formed so as to be in contact with the first metallic compound and the third metallic compound in common; and

a second main electrode formed on a second main surface opposite to the first main surface of the semiconductor substrate.

14. (Previously Presented): The semiconductor device according to claim 13, further comprising a second insulating film which is formed in the second area of the drift layer and on a further peripheral area surface of the terminating portion side end surface of the third metallic compound,

wherein the impurity diffused layer is formed in a self-alignment manner with respect to an end portion of the second insulating film on the cell portion side.

15. (Previously Presented): The semiconductor device according to claim 14, wherein the second insulating film is formed thicker than the first insulating film.

16. (Previously Presented): The semiconductor device according to claim 13, further comprising a second insulating film which is formed thicker than the first insulating film in the second area of the drift layer and outside of the third metallic compound,

wherein the impurity diffused layer is formed in a self-alignment manner with respect to an end portion of the second insulating film on the cell portion side.

17. (Previously Presented): The semiconductor device according to claim 13, wherein the second insulating film has a first side wall spacer formed on an end surface thereof on the cell portion side, and

the third metallic compound is formed in a self-alignment manner with respect to the first wall spacer.

18. (Previously Presented): The semiconductor device according to claim 13, further comprising a third insulting film which is formed on a surface of an end portion of the impurity diffused layer on the terminating portion side and has a thickness which allows passage of a second conductivity type impurity to form the impurity diffused layer.

19. (Previously Presented): The semiconductor device according to claim 13, wherein the control electrode is formed so as to have a stripe planar shape, and

a distance between an end surface of the third metallic compound on the terminating portion side and an end surface of the impurity diffused layer on the terminating portion side is assured by a diffusion depth of the impurity diffused layer in a direction orthogonal to a longitudinal direction of the stripe of the control electrode and a width of the first side wall spacer.

20. (Previously Presented): The semiconductor device according to claim 13, wherein a distance between the end surface of the third metallic compound on the terminating portion side and an end surface of the impurity diffused layer on the terminating portion side is equal to or more than 0.2 μm.

21. (Previously Presented): The semiconductor device according to claim 13, further comprising a second side wall spacer provided on a side surface of the control electrode,

wherein the first metallic compound and the second metallic compound are insulated from each other by the second side wall spacer.

22. (Previously Presented): The semiconductor device according to claim 21, wherein the second metallic compound is extended onto the second side wall spacer.

23. (Previously Presented): The semiconductor device according to claim 13, further comprising a fourth metallic compound formed on a top face of the field plate electrode.

24. (Previously Presented): The semiconductor device according to claim 14, wherein to the field plate electrode is applied substantially the same potential as that of the first main electrode or the control electrode.

25-44. (Canceled).